

Responding to paragraph 4 of the Office Action, the rejection of claims 1-2 and 4 under 35 U.S.C. 102(b) as being anticipated by Becker et al. (U.S. Patent No. 5,886,929, "Becker") is respectfully traversed.

The Examiner states that Becker discloses:

a synchronous portion comprising high speed latch 210, which is receiving and responding to system clock (SCLK);

an asynchronous portion coupled to output terminal 203 for the word lines of memory cell such as shown in Fig. 1 Prior Art;

feedback-resetting portion comprising: output feedback inverters 204 and 206 and power-up select unit 202a, set enable and disable unit 202b;

asynchronous reset signal RESET 224.

In spite of the Examiner's assertion, Becker teaches that output terminal 203 is synchronous, not asynchronous, with respect to latch 210. As explained at Col. 6, lines 10-13 and 27-34, output 203 goes high at time t4 in response to clock signal SCLK going high at time t2. Likewise, output 203 goes low at time t8 in response to clock signal SCLK going low at time t6. Thus, terminal is synchronous with clock signal SCLK and latch 210, not asynchronous.

In spite of the Examiner's assertion, the undersigned has been unable to find any feedback-resetting portion of Becker substantially isolating the synchronous portion from the asynchronous portion. In this regard, Claim 1 is limited to:

c. a feedback-resetting portion comprising an input receiving an input signal from the asynchronous portion and an output transmitting an output signal

to the synchronous portion in response to the input signal, the feedback-resetting portion substantially isolating the synchronous portion from the asynchronous portion responsive to an asynchronous reset signal.

As stated at Col. 5, lines 60-61, "line 222 is electrically coupled to output 203 as shown in FIG. 4C." Since output 203 is driven by clock signal SCLK as explained previously, line 222 also is driven by clock signal SCLK. Inverter 206 responds to the clock signal as explained at Col. 5, lines 56-65 and Col. 6, lines 31-44. Inverter 204 responds to the clock signal as explained at Col. 6, lines 10-30 and 46-51. Thus, the feedback-resetting portion of Becker asserted by the Examiner does not isolate latch 210 from terminal 203. In fact, output 203, inverter 206 and inverter 204 all respond to clock signal SCLK. Thus, Becker does not describe a feedback-resetting portion substantially isolating the synchronous portion from the asynchronous portion as claimed.

In spite of the Examiner's assertion, the undersigned has been unable to find any portion of Becker teaching that an asynchronous portion is responsive to an asynchronous reset signal. In this regard, claim 1 is limited to:

c. a feedback-resetting portion comprising an input receiving an input signal from the asynchronous portion and an output transmitting an output signal to the synchronous portion in response to the input signal, the feedback-resetting portion substantially isolating the synchronous portion from the asynchronous portion responsive to an asynchronous reset signal.

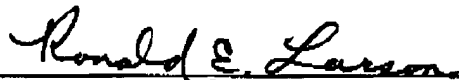
As explained previously, Invert r 204, which generates the reset signal, is synchronous with clock signal SCLK. Therefore, the reset signal is not asynchronous. Moreover, as explained at Col. 6, lines 26-30, when the RESET function is enabled, system clock CLK is capable of driving output 203 LOW by generating clock signal SCLK LOW. Thus, the RESET signal does not isolate a synchronous portion from an asynchronous portion, as claimed, but rather further enables clock signal SCLK to drive output 203, thereby ensuring that output 203 is synchronous with latch 210, which also is driven by clock signal SCLK. As a result, the reset signal of Becker does not substantially isolate a synchronous portion from an asynchronous portion as claimed.

Claims 2 and 4 are dependent on claim 1 and are allowable on the same grounds as claim 1. In addition, claim 2 is limited to isolating the synchronous portion from the asynchronous portion responsive to a monitor signal. The undersigned has been unable to find any portion of Becker teaching such a monitor signal.

In summary, each of claims 1-2 and 4 is allowable, and such action is respectfully requested.

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Respectfully submitted,



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